METHODS AND ARRANGEMENTS FOR AN ENHANCED SCANABLE LATCH CIRCUIT

ABSTRACT

Methods, and arrangements to enhance speed and reduce power consumption in a scanable latch circuit are disclosed. Embodiments include a wired-or circuit to facilitate independent paths for scan data and normal input data through the scanable latch circuit. In particular, to reduce delays related to gates between the input pin for the system clock and a normal input gate, dual, substantially independent paths are implemented: a scan path and a normal input path. Embodiments coordinate transmission of data from a normal input gate and a scan input gate to an output latch, a scan out pin, and/or combinational logic by incorporating buffers that isolate a wired-or node from either the scan input gate, the normal input gate, or both with a high impedance.